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(71) Applicant: **HITACHI LTD**

(72) Inventor: **SUZUKI TAKESHI**

(54) **SEMICONDUCTOR MEMORY DEVICE**

(57) Abstract:

PROBLEM TO BE SOLVED: To obtain a semiconductor memory device in which the power consumption of a memory array is reduced by a method wherein, when a word line inside the memory array is selected and driven, a dummy cell which is selected and driven simultaneously and which outputs a prescribed read signal is installed and the read signal is supplied to a driver circuit or a decoder circuit.

SOLUTION: In a precharging period, a bit line BL and a bit line -BL as well as a dummy bit line DBL and a dummy bit line -DBL are charged to VDD, the output of an inverter INV1 which is connected to the dummy bit line DBL is set to a low level, and a word line can be selected and driven. When the potential of the dummy bit line DBT, becomes lower than the threshold value of the inverter INV1, the output of the inverter INV1 is inverted, the output of a NOR gate G1 is set to the low level irrespective of a signal from a decoder 11, and the word line rises to a nonselection level. As a result, the fall timing of the word line becomes fast, and the time in which a current is made to flow to a memory cell in a selection state can be shortened.